Patent Claims

1. A semiconductor substrate having
a carrier substrate (1);
a semiconductor component layer (3); and
an insulation layer (2) which is formed between the carrier substrate (1) and the semiconductor component layer (3),
characterized by
a multiplicity of depressions (P) formed in the carrier substrate (1) in a surface facing the insulation layer (2),
a dielectric layer (D), which is formed at the surface of the multiplicity of depressions (P) and of the carrier substrate (1); and
an electrically conductive layer (E2), which is formed at least in the multiplicity of depressions (P) for realizing a multiplicity of capacitor electrodes,
a further electrically conductive layer being formed in the carrier substrate (1) for realizing capacitor counterelectrodes (E1) at least in the region of the depressions.

2. The semiconductor substrate as claimed in patent claim 1, characterized in that the electrically conductive layer (E2) is also formed at the surface of the carrier substrate (1) and connects together a group of the multiplicity of capacitor electrodes for realizing group capacitors (PK).

3. The semiconductor substrate as claimed in patent claim 2, characterized in that the group capacitors (PK) have a capacitance of approximately 30 fF.

4. The semiconductor substrate as claimed in one of patent claims 1 to 3, characterized in that the depressions (P) represent pores formed by electrochemical pore etching.

5. The semiconductor substrate as claimed in one of patent claims 1 to 4, characterized in that the carrier substrate (1) has a semiconducting material, the capacitor counterelectrode (E1) representing a doping region formed in the semiconductor material, or a conductive material.

6. The semiconductor substrate as claimed in one of patent claims 1 to 5, characterized in that the dielectric layer (D) has a high-temperature-resistant capacitor dielectric with a high dielectric constant.

7. The semiconductor substrate as claimed in one of patent claims 1 to 6, characterized in that the electrically conductive layer (E2) has doped polycrystalline semiconductor material.

8. The semiconductor substrate as claimed in one of patent claims 1 to 7, characterized in that
it has an SOI substrate having
a monocrystalline Si layer as semiconductor component layer (3);
an SiO_2 layer as insulation layer (2);
a poly-Si-layer as electrically conductive layer (E2); and
an Si substrate as carrier substrate (1).

9. A method for fabricating a semiconductor substrate having the following steps:
a) formation of a multiplicity of depressions (P) and a capacitor counterelectrode (E1) in a carrier substrate (1);
b) formation of a dielectric layer (D) at the surface of the depressions (P) and of the carrier substrate (1);
c) formation and patterning of an electrically conductive layer (E2) on the dielectric layer (D) for realizing a multiplicity of capacitor electrodes at least in the multiplicity of depressions (P);

d) formation of a first insulation partial layer (2A) at the processed surface of the carrier substrate (1);
e) provision of a semiconductor component substrate (3) with a splitting-off boundary layer (3S), and a second insulation partial layer (2B);
f) connection of the semiconductor component substrate (3) and the carrier substrate (1) at their insulating partial layers (2A, 2B) to form an insulation layer (2); and
g) splitting off part of the semiconductor component substrate (3) at the splitting-off boundary layer (3S).

10. The method as claimed in patent claim 9, characterized in that, in step a),
a1) an electrochemical pore etching is carried out for forming pores (P) as depressions in a semiconductor substrate (1); and
a2) a doping of the semiconductor substrate (1) is carried out in the vicinity of the pores (P) for forming a further electrically conductive layer as capacitor counterelectrode (E1).

11. The method as claimed in patent claim 10, characterized in that, in step a2),
a21) a formation of a doping glass is carried out at least in the pores (P);
a22) a thermal treatment is carried out; and
a23) a wet-chemical removal of the doping glass is carried out.

12. The method as claimed in one of patent claims 9 to 11, characterized in that, in step b), a high-temperature-resistant capacitor dielectric with a high dielectric constant is formed over the whole area.

13. The method as claimed in patent claim 12, characterized in that nitrided oxide, Al_2O_3 and/or TiO_2 is formed as the capacitor dielectric.

14. The method as claimed in one of patent claims 9 to 13, characterized in that, in step c),
c1) an electrically conductive layer (E2) is formed for filling the depressions (P) over the whole area; and
c2) the electronically conductive layer (E2) is at least partially or completely removed as far as the dielectric layer (D) at the surface of the carrier substrate (1).

15. The method as claimed in patent claim 14, characterized in that, in step c1),
in-situ-doped polysilicon is deposited; and
in step c2),
photolithographic patterning with an isotropic etching-back is carried out in such a way that a multiplicity of capacitor electrodes are connected to one another for realizing a group capacitor (PK).

16. The method as claimed in one of patent claims 9 to 15, characterized in that, in step d),
a TEOS deposition method is carried out.

17. The method as claimed in one of patent claims 9 to 16, characterized in that, in step e),
a semiconductor wafer (3) with an oxide layer (2B) is provided, the splitting-off boundary layer (3S) being formed by means of hydrogen implantation.

18. The method as claimed in one of patent claims 9 to 17, characterized in that, in step f),
the connection is carried out by means of wafer bonding.

19. The method as claimed in one of patent claims 9 to 18, characterized in that, in step g),
the splitting off is carried out by means of a further thermal treatment.

20. A semiconductor circuit in a semiconductor substrate as claimed in one of patent claims 1 to 8, characterized by
a semiconductor component (4, 5, 6, 7, 8) formed in the semiconductor component layer (3);
a contact hole (V), formed at least in the insulation layer (2); and
a connecting layer (9), which connects the semiconductor component (4, 5, 6, 7, 8) to at least one of the capacitor electrodes (E2) via the contact hole (V).

21. The semiconductor circuit as claimed in patent claim 20, characterized in that it represents a DRAM memory cell having a selection transistor (AT) and a capacitor (PK).

22. A method for fabricating a DRAM memory cell in a semiconductor substrate as claimed in one of patent claims 1 to 8 or a semiconductor substrate fabricated as claimed in patent claims 9 to 19, having the following steps:
a) formation of a shallow trench isolation in the semiconductor component layer (3) for realizing active regions;
b) formation of a selection transistor (AT) having source/drain regions (7), a gate dielectric (4), a control layer (5) serving as wordline (WL), and a gate insulation (6, 8);
c) formation of a contact hole (V) at least in the insulation layer (2) and the semiconductor component layer (3);
d) formation of a connecting layer (9) in the contact hole (V) between a source/drain region (7) of the selection transistor (AT) and at least one capacitor electrode (E2);
e) formation of an intermediate insulation layer (10) with a bitline contact (11) to a complementary source/drain region (7); and

f) formation and patterning of a bitline layer (12) for realizing a bitline (BL) at the surface of the intermediate insulation layer (10).

23. The method as claimed in patent claim 22, characterized in that, in step c),
the contact hole (V) is etched free in a self-aligning manner using the gate insulation (6, 8) and a lithographic method.

24. The method as claimed in patent claim 22 or 23, characterized in that, in step d),
in order to form the connecting layer (9), a further in-situ-doped polycrystalline semiconductor layer is deposited over the whole area and subsequently etched back isotropically or anisotropically.